**REPORT ON "Experimental Analysis of MOS Capacitor for Oxide Furnaces by using CV Plotter Metrology and Identification of Fabrication Facilities and their Processes"**

at

**SEMICONDUCTOR LABORATORY MOHALI (PUNJAB),**

**MINISTRY OF ELECTRONICS & INFORMATION TECHNOLOGY**

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**(AnAutonomous CollegeUnder UGCACT)**

# <u>CERTIFICATE</u>

This is to certify that the project work titled **“EXPERIMENTAL ANALYSIS OF MOS CAPACITOR FOR OXIDE FURNACES BY USING CV PLOTTER METROLOGY AND IDENTIFICATION OF FABRICATION FACILITIES AND THEIR PROCESSES ”** being submitted by **Adarsh Mishra** is the midterm report to partial fulfilment of the requirement for the award of **Bachelor of Technology** degree and is record of bona fide work done under my guidance.

**Mr. Dheeraj Deeconda**

**Sci/Engr., SCL**

## GURU NANAK DEV ENGINEERING COLLEGE, LUDHIANA

## CANDIDATE'S DECLARATION

I Adarsh Mishra hereby declare that I have undertaken one month training at Semi-Conductor Laboratory, Mohali during a period from 10 July 2023 to 04 August 2023 in partial fulfilment of requirements for the award of degree of B.Tech. (Electronics and Communication Engineering) at GURU NANAK DEV ENGINEERING COLLEGE, LUDHIANA. The work which is being presented in the training report submitted to Department of Electronics and Communication Engineering at GURU NANAK DEV ENGINEERING COLLEGE, LUDHIANA is an authentic record of training work.

Signature of the Student

The one-month industrial training Viva-Voce Examination of has been held on and accepted.

Signature of Internal Examiner Signature of External Examiner

// Abstract

Very Large-Scale Integration (VLSI) fabrication has made significant strides in recent years, with various parts of the world playing important roles in the production of semiconductors. This study explores the capabilities, infrastructure, and significant technological advancements of VLSI fabrication labs in China, Taiwan, the United States, and Europe. The study identifies the strengths and weaknesses of each region, shedding light on their competitive advantage in the semiconductor sector, through a thorough review of the literature and industry reports.

The study also focuses on the Capacitance-Voltage (CV) analysis for Metal-Oxide-Semiconductor (MOS) capacitors, which is a crucial component of VLSI technology. In order to accurately characterizecapacitance and charge distribution, the project examines how MOS capacitors behave under various voltage conditions.

This study contributes to a better understanding of the technological landscape in these regions and aids in the identification of potential collaborative opportunities and best practises by combining the findings from the comparative analysis of VLSI fabrication facilities and the investigation of CV analysis for MOS capacitors. The findings are intended to support technological development and strengthen global cooperation in the semiconductor industry by providing information to policymakers, industry stakeholders, and researchers alike.

## ACKNOWLEDGMENT

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# About Semi-Conductor Laboratory

## About SCL

Semi-Conductor Laboratory (SCL) is an autonomous body under Ministry of Electronics & Information Technology, Government of India. SCL has integrated facilities / supporting infrastructure all under one roof and undertakes activities focused on Design, Development, Fabrication, Assembly & Packaging, Testing and Quality Assurance of complementary metal oxide semiconductor (CMOS) and micro-electro mechanical systems (MEMS) devices for various applications. SCL has over the years developed and supplied a number of key VLSIs, majority of which have been Application Specific Integrated Circuits (ASICs) for high reliability applications in industrial and space sectors. Steps have been initiated to upgrade the facilities to fabricate devices in 0.25 micron or better technology. The Semi-Conductor Laboratory is responsible for design and development of very-large-scale integration (VLSI) devices and development of systems for telecommunication and space sectors. SCL has facilities for fabrication of CMOS devices in 0.18 micrometre range and Micro Electro Mechanical Systems. Production Lots at SCL are being processed with Application Specific Integrated Circuits (ASICs)/Test Chips designed inhouse. There is ever-increasing requirement of incorporating more features and reducing size, weight and volume of on-board systems coupled with improved reliability through higher level of integration.

## Departments in SCL

- VLSI & MEMS fabrication Group (VMFG)
- Design and Process Group (DPG)
- Packaging and Testing
- System Assembly
- Reliability & Quality Assurance(R&QA)

# LIST OF ABBREVIATIONS

- **CMOS**: Complementary Metal Oxide Semiconductor
- **MOSFET**: Metal Oxide Semiconductor Field Effect Transistor
- **VLSI**: Very Large Scale Integrated
- **CMP**: Chemical Mechanical Polishing
- **CVD**: Chemical Vapor Deposition
- **PVD**: Physical Vapor Deposition
- **SEM**: Scanning Electron Microscope
- **APCVD**: Atmospheric Pressure CVD
- **LPCVD**: Low Pressure CVD
- **PECVD:** Plasma Enhanced CVD
- **CD**: Critical Dimension

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# CHAPTER 1
# INTRODUCTION TO VLSI

## 1.1 Overview of VLSI

VLSI (Very Large-Scale Integration) is a field that revolves around designing and fabricating integrated circuits with an enormous number of transistors packed onto a single chip. This technology involves various crucial activities such as IC design, utilizing EDA (Electronic Design Automation) tools for simulation and verification, IC fabrication, and adhering to Moore's Law to scale down the size of transistors. The magic of VLSI lies in its ability to integrate entire systems onto a single chip, commonly known as System-on-Chip (SoC), which finds applications in numerous industries like consumer electronics, telecommunications, automotive, healthcare, and more. However, VLSI design presents several challenges that designers must address to create efficient and powerful electronic systems. Some of these challenges include optimizing power consumption, managing heat dissipation, ensuring signal integrity, achieving precise timing closure, ensuring manufacturability, and devising effective testing methodologies. Despite these challenges, VLSI has revolutionized the electronics industry, driving innovation, and enabling the development of increasingly sophisticated electronic systems. Its impact on technology is far-reaching, and it continues to shape the future of electronics.

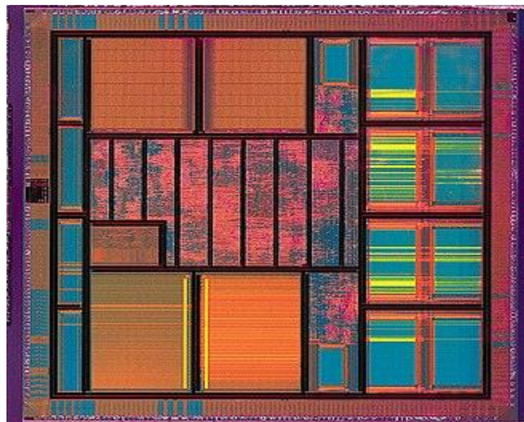


Fig 1.1: A VLSI Integrated circuit die

## 1.2 Silicon Wafer

A silicon wafer is a vital building block for the production of integrated circuits (ICs) and other semiconductor devices. Its manufacturing involves a series of precise steps:

1. Silicon Ingot Growth: The process begins with high-purity silicon melted and solidified into a cylindrical crystal ingot.

2. Ingot Slicing: Using diamond-edged or wire saws, the ingot is sliced into thin wafers with specific thicknesses, typically ranging from 150 micrometres to a few millimetres.

3. Grinding and Polishing: Sliced wafers undergo grinding and polishing to achieve a smooth, flat surface, eliminating any irregularities from slicing.

4. Cleaning: Thorough cleaning ensures removal of contaminants or particles from the wafer surfaces.

5. Thermal Oxidation: In some cases, the cleaned wafers undergo thermal oxidation at high temperatures to form a thin silicon dioxide ($SiO_2$) layer on the surface, providing desirable properties.

6. Dopant Introduction: Dopants, intentional impurities, are introduced into the wafers through processes like ion implantation or diffusion. This creates regions with different conductivity types (e.g., n-type or p-type) on the wafer.

Silicon wafers serve as the crucial foundation for depositing and patterning multiple layers of electronic components, enabling the creation of advanced and compact semiconductor devices.

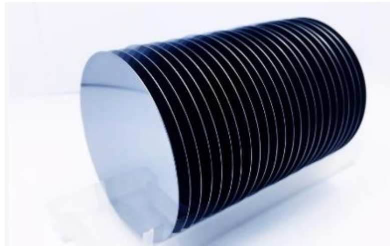


Fig 1.2: Silicon Wafers 8' inch

## 1.3 IC Fabrication Process Flow

The IC fabrication process flow involves the following key steps:

1. Wafer Preparation: Silicon wafers are meticulously cleaned and polished to achieve a smooth surface.

2. Photolithography: A layer of photoresist is applied to the wafer, and a photomask is used to transfer the circuit pattern onto the wafer.

3. Etching: Unwanted material is selectively removed from the wafer using either wet or dry etching processes.

4. Doping: Specific regions of the wafer are infused with impurities to modify their electrical properties.

5. Deposition: Thin layers of materials, such as dielectrics and metals, are deposited on the wafer to create various components and interconnects.

6. Lithography and Patterning: Additional layers of photoresist are applied, and patterns are defined through lithography and etching, creating a multi-layered structure.

7. Metallization: Contacts and vias are formed to establish electrical connections between different layers of interconnect, and metal layers are patterned to define interconnect routes.

8. Backend Processes: The wafer undergoes passivation with protective layers, chips are bonded to packages, rigorous testing is performed to ensure functionality, and final packaging is completed.

These steps in IC fabrication are crucial in creating intricate semiconductor devices that power modern electronics.

Fig 1.3: Process Flow of IC Fabrication

# CHAPTER 2

# CLEAN ROOM

## 2.1 Contamination Types

Contamination is the introduction of undesirable substances or particles that can have detrimental effects on product quality, performance, or process reliability. In various industries and cleanroom environments, different types of contamination can occur, including:

1. Particulate Contamination: This involves the presence of solid particles in the air or on surfaces, such as dust, fibers, lint, and other debris.

2. Chemical Contamination: Unwanted chemicals or substances may be present, adversely affecting products or processes. Examples include cleaning agents, solvents, or residues from previous processes.

3. Microbial Contamination: This refers to the presence of microorganisms like bacteria, fungi, or viruses, which can pose significant risks to product safety and integrity, especially in industries like pharmaceuticals or biotechnology.

4. Electrostatic Discharge (ESD): Occurs when there is a sudden transfer of electric charge between objects with different electrical potentials, potentially damaging sensitive electronic components.

5. Cross-Contamination: This occurs when contaminants are transferred between different surfaces, materials, or products, leading to unintended contamination and potential compromises in quality or safety.

Addressing and controlling these various types of contamination are critical for maintaining high product quality and ensuring the reliability of industrial processes.

Fig 2.1: Clean room

## 2.2 Cleanroom Protocols

Cleanroom protocols are a set of guidelines and procedures designed to uphold cleanliness, control contamination, and preserve the integrity of products and processes within a cleanroom environment. These protocols encompass several key aspects:

1. Entry and Exit Procedures: Strict measures are in place for entering and exiting the cleanroom, including proper gowning procedures and the use of air showers or airlocks to remove particles from personnel before entry.

2. Behavior and Conduct: Cleanroom personnel adhere to appropriate behavior, such as following designated paths, minimizing movement, and avoiding actions that could generate particles and introduce contaminants.

3. Material and Equipment Handling: Careful handling of materials and equipment is emphasized, using cleanroom-compatible tools, containers, and packaging to prevent contamination during transportation and usage.

4. Cleaning and Disinfection: Regular cleaning and disinfection protocols are followed to maintain the cleanliness of surfaces, equipment, and workstations within the cleanroom. Suitable agents and techniques are employed to ensure the environment remains free from contaminants.

5. Maintenance and Monitoring: Cleanroom systems undergo routine maintenance, including air filtration and HVAC system checks. Continuous monitoring of critical parameters, such as particle count, temperature, humidity, and air pressure differentials, is conducted to ensure the environment remains controlled.

By diligently adhering to cleanroom protocols, organizations can effectively minimize the presence of contaminants, sustain a controlled environment, and uphold the high quality and reliability of products and processes within the cleanroom setting.

Fig 2.2: Clean Room Protocols

# CHAPTER 3

# VLSI FABRICATION PROCESSES

## 3.1 Diffusion

**Diffusion** is a crucial process in semiconductor manufacturing that involves the controlled movement of dopant atoms into a semiconductor material to create specific regions with desired electrical properties. This step is essential for producing transistors, diodes, and other components in integrated circuits (ICs).

Various techniques are employed for diffusion, with one of them being oxidation. Oxidation entails growing a thin layer of oxide on the surface of the semiconductor material, commonly silicon. In this process, the semiconductor material is exposed to oxygen or water vapor at high temperatures, resulting in a chemical reaction that forms an oxide layer. This oxide layer acts as a barrier, preventing the diffusion of dopant atoms through it. However, it is possible to control the process parameters to introduce dopant atoms into the oxide layer itself, creating doped oxide regions.

There are two primary types of oxidation processes:

I. Dry Oxidation: This method utilizes a high-temperature furnace with a pure oxygen (O2) ambient. Oxygen molecules dissociate into oxygen atoms, which then directly react with silicon to form SiO2. Dry oxidation is conducted at higher temperatures, leading to slower oxidation rates. The result is higher-quality oxide layers with lower defect densities and improved electrical properties. This type of oxidation is commonly used for critical applications, such as forming gate oxide in MOS transistors.

II. Wet Oxidation: Wet oxidation involves using a water vapor (H2O) ambient at lower temperatures. At elevated temperatures, water vapor dissociates into hydrogen (H2) and oxygen (O2). The oxygen atoms then react with silicon to form SiO2. Wet oxidation occurs at lower temperatures, resulting in faster oxidation rates. However, it typically yields oxide layers with lower quality, higher defect densities, and reduced electrical properties compared to dry oxidation. As a result, it is often used for non-critical applications where high-quality oxide layers are not essential.

2. **Annealing:** Annealing is a heat treatment process used in IC fabrication to relieve stress, activate dopant atoms, and enhance material properties. It involves heating the semiconductor material to a specific temperature and holding it for a predetermined time. Annealing promotes dopant diffusion, enabling the creation of desired dopant profiles. It helps remove defects and lattice damage, making dopants electrically active.

Types of furnaces commonly used in industrial processes for the heat treatment and processing of materials:

a. Alloy Furnace: An alloy furnace, also known as a melting furnace or smelting furnace, is specifically designed for melting and alloying different metals or metallic alloys. It is used to combine and melt various metal components to create a homogeneous mixture or alloy with specific desired properties. The alloy furnace typically operates at high temperatures to facilitate the melting and homogenization of metals, allowing for precise control over the composition of the resulting alloy. It is used for layers of Aluminium.

b. Sinter Furnace: A sintering furnace is utilized in the process of sintering, which involves compacting and heating powdered materials to form a solid mass without reaching the melting point of the materials. The sintering furnace facilitates the bonding of particles within the material, resulting in increased strength, density, and improved mechanical properties. The furnace typically operates at temperatures below the melting point of the material but high enough to induce diffusion and consolidation. Sintering furnaces may utilize various heating methods such as electric resistance heating, radiant heating, or microwave heating, depending on the specific requirements of the sintering process.

3. **LPCVD:** LPCVD stands for Low-Pressure Chemical Vapour Deposition. It is a widely used technique in IC fabrication for depositing thin films of various materials onto semiconductor substrates. LPCVD operates at reduced pressures compared to atmospheric pressure, allowing for better control over the deposition process. There are three types of furnaces used in LPCVD:

a. Nitrate Furnace: A nitrate furnace, also known as a nitridation furnace, is used for the nitridation process in semiconductor fabrication. Nitridation involves the introduction of nitrogen into the surface of a silicon substrate to form a thin silicon nitride ($Si_3N_4$) layer. The nitrate furnace provides a controlled environment for the reaction between silicon and nitrogen-containing gases, such as ammonia ($NH_3$), to form the silicon nitride layer.

The silicon nitride layer serves as a dielectric material with excellent electrical insulating properties and is commonly used in device isolation, Passivation layers, and gate dielectrics.

b. Poly Furnace: A poly furnace, short for polysilicon furnace, is used for the deposition and annealing of polysilicon (polycrystalline silicon) thin films. Polysilicon is a material composed of multiple small silicon crystals, and it exhibits unique electrical properties, including low resistivity and compatibility with silicon processing. The poly furnace allows for the deposition of polysilicon layers using various methods such as LPCVD (Low-Pressure Chemical Vapour Deposition) or PECVD (Plasma-Enhanced Chemical Vapour Deposition). Additionally, it provides high-temperature annealing to enhance the electrical conductivity and control the grain size of the polysilicon, which is crucial for applications like gate electrodes, interconnects, and resistors in integrated circuits.

c. TEOS Furnace: TEOS, or Tetraethyl Orthosilicate, is a silicon source material used in the deposition of silicon dioxide (SiO2) films by the CVD (Chemical Vapour Deposition) process. TEOS is a liquid precursor that is vaporized and then reacts with oxygen (O2) or water vapour (H2O) in a deposition chamber to form a layer of silicon dioxide. TEOS-based CVD is commonly utilized for depositing high-quality SiO2 films with excellent electrical properties and conformal coverage on complex substrate topographies. The deposited SiO2 films find applications in various areas such as insulation layers, inter-metal dielectrics, and capacitor dielectrics in semiconductor devices.

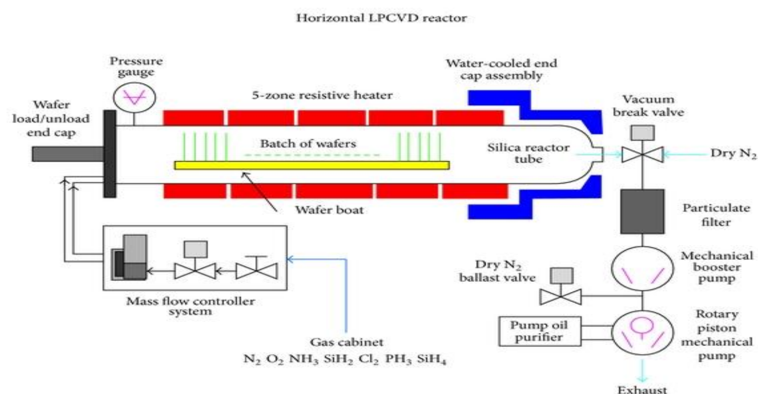



Fig 3.1: LPCVD Process

Several meteorological tools used in diffusion process are-

a. **Ellipsometer:** An ellipsometer is an instrument commonly used in IC fabrication and semiconductor research to measure the thickness and optical properties of thin films. It is based on the principle of ellipsometry, which involves measuring changes in the polarization state of light reflected from a sample surface.

b. **CV Plot:** CV plot stands for Capacitor Voltage plot. This plot is used to characterize the electrical behaviour of a semiconductor device, typically a diode or a MOS structure. A CV plot represents the capacitance of the device as a function of the applied voltage. It is obtained by measuring the capacitance at different bias voltages while keeping the frequency constant. The plot helps in understanding the charge storage and carrier concentration within the device.

c. **Laser marker:** A laser marker, also known as a laser marking system or laser engraver, is a device that uses laser technology to create permanent marks, engravings, or surface modifications on various materials. Here it is used to mark identity on Silicon wafer.

d. **Quartz Cleaner:** Quartz cleaners are designed to remove contaminants, such as particles, organic residues, and films, from quartz ware to ensure optimal performance and longevity.

## 3.2 Photolithography

Photolithography plays a critical role in semiconductor fabrication, allowing intricate patterns to be transferred onto a semiconductor substrate. The process involves utilizing light, a photosensitive material called photoresist, and a series of steps to define the desired features on the substrate. Here is a concise overview of the steps involved:

1. Substrate Preparation: The semiconductor substrate, typically a silicon wafer, undergoes thorough cleaning and preparation to ensure optimal adhesion of subsequent layers. This may involve cleaning, priming, and applying adhesion promoters.

2. Photoresist Application: A thin layer of photosensitive material called photoresist is spin-coated onto the substrate. The photoresist is sensitive to light and undergoes chemical changes upon exposure.

3. Alignment and Masking: A mask or photomask, containing the desired pattern, is aligned to the wafer using alignment marks. The mask is placed in close proximity to the coated wafer to achieve precise alignment for accurate pattern transfer.

4. Exposure: The aligned wafer and mask are exposed to ultraviolet (UV) light. The light passes through the transparent areas of the mask, exposing the underlying photoresist. This UV light triggers a chemical reaction that alters the solubility of the photoresist in the exposed regions.

5. Development: After exposure, the wafer undergoes a post-exposure bake step to stabilize the chemical changes in the photoresist and enhance pattern definition. The exposed wafer is then immersed in a developer solution that selectively removes either the exposed regions (positive photoresist) or unexposed regions (negative photoresist). This step reveals the desired pattern on the wafer.

6. Hard Bake: To further stabilize the patterned photoresist, a hard bake step is performed. The wafer is heated to a higher temperature, ensuring complete curing and improving the durability of the developed photoresist. The patterned photoresist acts as a mask for subsequent etching processes.

7. Etching: The exposed areas of the substrate not protected by the patterned photoresist are etched, selectively removing material to transfer the pattern onto the underlying layers.

8. Resist Stripping: Once the pattern transfer is complete, the remaining photoresist is removed from the wafer. Resist stripping can be achieved through chemical processes, plasma treatments, or a combination of methods, leaving behind the desired pattern on the substrate.

These steps are repeated for each layer of the integrated circuit, allowing precise definition and replication of patterns necessary for device functionality.

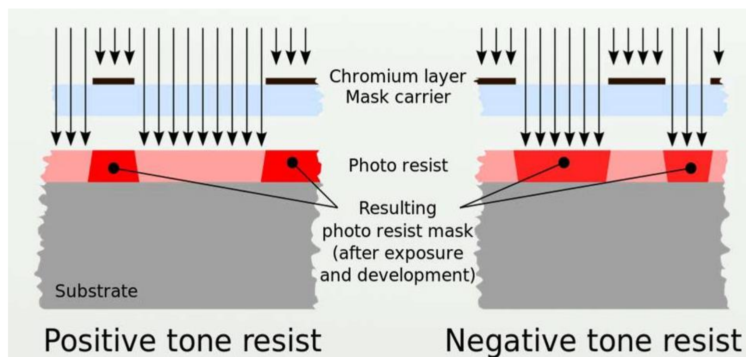



Fig 3.2: Types of Photoresists

## 3.3 Thin Film

Thin film refers to a layer of material that has a thickness ranging from a few nanometers to several micrometers. It is typically deposited onto a substrate using various techniques, such as physical vapour deposition (PVD), chemical vapour deposition (CVD), or sputtering.

i. **CVD**: CVD stands for Chemical Vapour Deposition, which is a widely used technique for depositing thin films onto substrates. In CVD, a chemical reaction occurs in a gas phase, where precursor molecules are introduced and react to form a solid film on the substrate surface. Types of CVD:

    a. Thermal CVD: In thermal CVD, the precursor molecules are thermally activated by heating to initiate the chemical reactions at the substrate surface.

    b. Plasma-Enhanced CVD (PECVD): In PECVD, a plasma is used to energize the precursor molecules, breaking them down into reactive species that can more readily participate in the chemical reactions. Plasma can be generated by applying radiofrequency (RF) or microwave power to the gas mixture.

    c. Low-Pressure CVD (LPCVD): LPCVD operates at reduced pressures, typically in the range of millitorr to torr. The lower pressure facilitates better control over the deposition process and allows for higher-quality films.

    d. Atmospheric Pressure CVD (APCVD): APCVD operates at ambient or near-ambient pressures, simplifying equipment requirements and enabling higher throughput. However, it generally results in lower-quality films compared to LPCVD.

ii. **PVD**: PVD stands for Physical Vapour Deposition, which is a thin film deposition technique that involves the physical transfer of material from a source to a substrate. Unlike chemical reactions as in CVD, PVD operates based on physical processes such as evaporation or sputtering to deposit the thin films. In evaporation-based PVD, a solid material is heated in a vacuum chamber, causing it to vaporize and form a vapour or gaseous phase. The vaporized material then condenses onto the substrate, forming a thin film as it cools. The evaporated material can be generated using techniques like resistive heating, electron beam evaporation, or flash evaporation. Sputtering-based PVD involves

bombarding a target material with high-energy ions, typically from plasma. The ion bombardment dislodges atoms or molecules from the target, which are then deposited onto the substrate. Sputtering can be performed using various methods such as DC sputtering, RF sputtering, magnetron sputtering, or reactive sputtering.

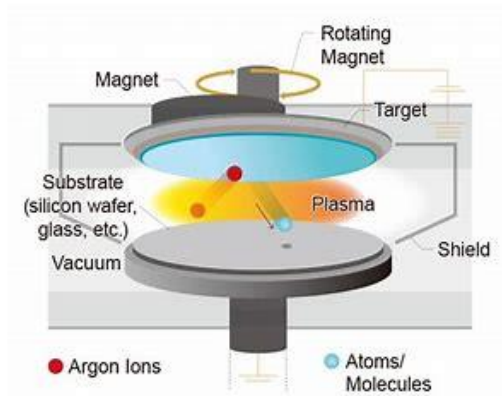



Fig 3.3: Sputtering

## 3.4 Ion Implantation

Ion implantation is a crucial semiconductor manufacturing process used to introduce impurity ions into a semiconductor substrate, altering its physical and electrical properties in a controlled manner. The process consists of several well-defined steps:

a) Ion Species Selection: The specific ion species are carefully chosen based on the desired doping characteristics and the requirements of the semiconductor device being fabricated.

b) Ion Source and Acceleration: An ion source generates the selected ion species, which can be a gas discharge source or a plasma source. These ions are then accelerated to high energies using an electrostatic or electromagnetic accelerator.

c) Ion Beam Shaping: The ion beam is shaped and controlled using magnetic fields or electrostatic lenses, ensuring a focused and precisely shaped ion beam for implantation.

d) Substrate Preparation: The semiconductor substrate, typically a silicon wafer, is prepared through cleaning and possibly pre-doping processes, ensuring an appropriate surface for ion implantation.

e) Implantation Parameters Selection: Crucial parameters like ion energy, ion dose (number of ions per unit area), implant angle, and temperature are carefully chosen based on the desired doping profile.

f) Ion Implantation: The high-energy ion beam is directed towards the substrate, and the ions penetrate the surface. Upon collision with lattice atoms, the ions come to rest, introducing dopant atoms and creating lattice defects.

g) Dose Monitoring: Throughout the implantation process, the ion dose is meticulously monitored and controlled to achieve the intended doping concentration.

h) Post-Implantation Annealing: After ion implantation, the substrate may undergo annealing processes to repair lattice damage caused by ion impacts and activate the dopant atoms. Annealing redistributes dopants within the lattice, optimizing their electrical properties.

i) Metrology and Quality Control: Implantation wafers undergo various metrology and quality control techniques, such as sheet resistance measurements, secondary ion mass spectrometry (SIMS), and electrical characterization. These methods verify the success of the implantation process and assess the resulting doping profile.

Ion implantation is a versatile and critical step in semiconductor manufacturing, enabling the precise doping necessary to create functional semiconductor devices.

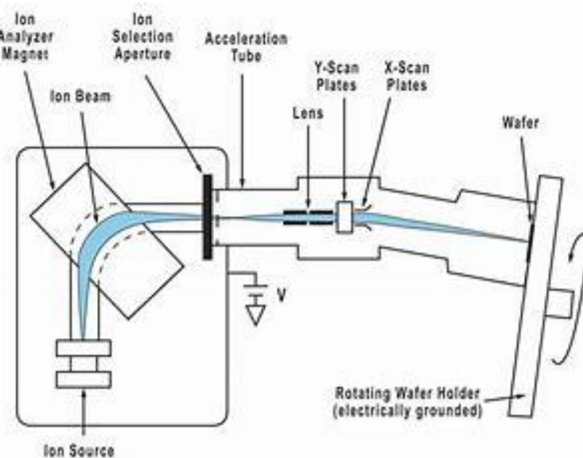



Fig 3.4: Ion Implantation process

- Difference between diffusion and ion implantation is shown below:

| DIFFUSION | ION IMPLANTATION |
|---|---|
| Diffusion relies on the natural movement of atoms driven by concentration gradients at elevated temperatures. | Ion implantation involves physically bombarding the substrate with high-energy ions. |
| Diffusion provides a more gradual and less precise doping profile. | Ion implantation offers greater control over dopant depth and concentration, precise patterning capabilities, and well-defined doping profiles. |
| Diffusion does not require an additional activation step after implantation. | Ion implantation requires an additional activation (thermal activation) step after implantation. |

Table 3.1 – Diffusion vs Ion Implantation

## 3.5 CMP

CMP stands for Chemical Mechanical Polishing, which is a process used in semiconductor manufacturing and other industries to planarize and smooth surfaces of wafers, substrates, or thin films. It involves simultaneous chemical and mechanical actions to remove material and achieve a flat, smooth surface. CMP is primarily used to create a planar surface by removing excess material and achieving uniform thickness across a substrate. It is commonly employed in various stages of semiconductor device fabrication, such as interlayer planarization, shallow trench isolation, or metal layer planarization. The CMP process involves three main components:

- Polishing Pad: A rotating polishing pad made of a polymeric material with a textured surface. It provides the mechanical action during polishing.
- Slurry: A mixture of abrasive particles suspended in a chemical solution. The slurry assists in material removal by abrasion and chemical reactions.
- Carrier: The carrier holds and transports the wafer or substrate against the rotating pad during polishing. It applies controlled pressure and ensures even distribution of the slurry.

Process Steps:

1. Wafer Loading: The substrate or wafer is mounted onto a carrier and secured in place.
2. Polishing: The carrier with the wafer is pressed against the rotating polishing pad, and the slurry is dispensed onto the pad. The combined mechanical and chemical action of the pad and slurry removes material from the wafer surface.
3. Post-Polishing Cleaning: After polishing, the wafer undergoes cleaning processes to remove any residual slurry and contaminants.

CMP involves both mechanical and chemical material removal mechanisms:

- Mechanical: The abrasive particles in the slurry physically abrade the surface, causing material removal through abrasion and friction.
- Chemical: The chemical components of the slurry can react with the surface material, forming complexes or undergoing chemical reactions to assist in material removal.

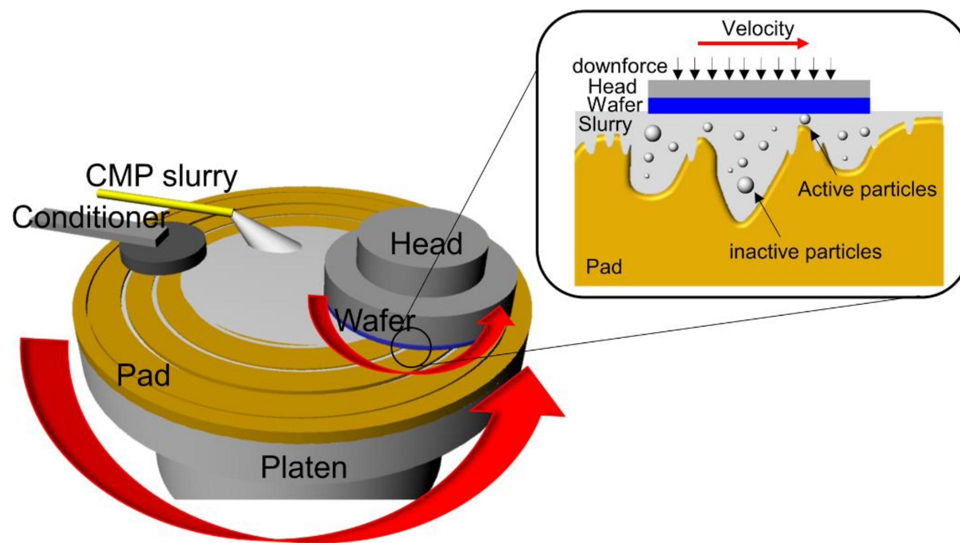



Fig 3.5: Chemical mechanical polishing

Advantages of CMP:

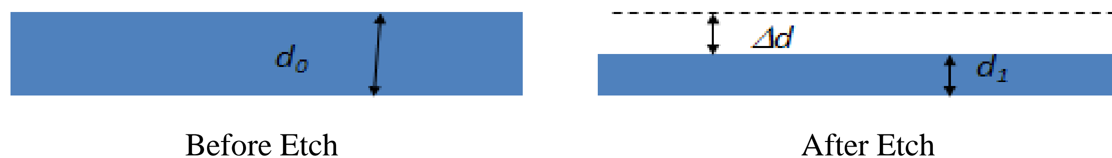
- CMP ensures a flat and smooth surface by removing high spots, bumps, and uneven layers. This improves device performance, reduces electrical leakage, and enhances interconnect reliability.
- CMP allows precise control over the thickness of deposited films and layers, ensuring uniformity across the wafer. This control is vital for maintaining device integrity and functionality.

- CMP can selectively remove specific materials while preserving underlying layers. This enables the removal of unwanted materials without damaging sensitive structures.
- CMP can achieve polishing at sub-micron levels, enabling the fabrication of high-resolution devices and tight dimensional control.
- MP seamlessly integrates with other semiconductor fabrication processes, making it compatible with various steps in the manufacturing flow.
- CMP can be applied to a wide range of materials, including metals, oxides, nitrides, and polymers. It enables uniform and controlled material removal across different materials.

## 3.6 Etching

Etching is a process used in semiconductor manufacturing and other industries to selectively remove material from the surface of a substrate. It involves the use of chemical or physical means to dissolve or erode specific regions of a material, creating patterns, structures, or features. Etching serves various purposes, including pattern transfer, material removal, surface modification, and device fabrication. It is commonly used to create features such as trenches, vias, channels, or interconnects on semiconductor wafers.

- Etch Rate: Etch rate refers to the speed at which the material is removed during etching. It can be controlled by adjusting factors such as etchant concentration, temperature, and process time.




Before Etch After Etch

Fig 3.6 (a): Etch Rate

- Selectivity: Selectivity is the ratio of the etch rates between the target material and the etch mask or other materials, allowing for precise material removal.
- Etch Uniformity: Etch uniformity refers to the degree of consistency in the etching process across a substrate or wafer. It measures how evenly the material is removed from the surface, ensuring uniformity in the etch depth, profile, and feature dimensions.

- Isotropic Etching: Isotropic etching refers to the etching process where material is removed uniformly in all directions, resulting in a roughly spherical or rounded etch profile. In this type of etching, the etchant attacks the material equally in all directions, without any preferential direction or selectivity. As a result, the etch rate is uniform across the entire exposed surface.
- Anisotropic Etching: Anisotropic etching refers to the etching process where material is preferentially removed in a specific direction or along certain crystallographic planes. Unlike isotropic etching, anisotropic etching produces non-uniform etch rates in different directions, resulting in distinct etch profiles with well-defined angles.

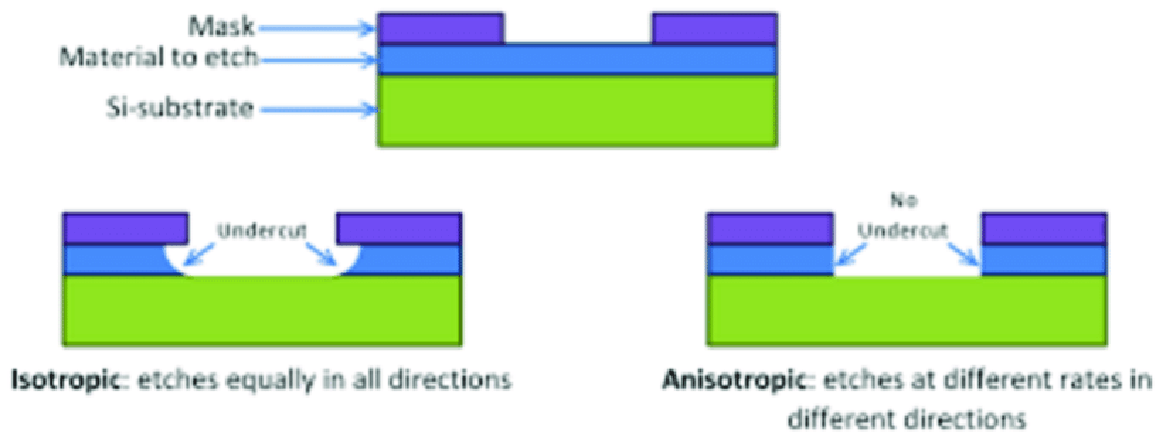



Fig 3.6 (b): Isotropic and Anisotropic Etching

There are two types of etching process:

I. Wet Etching: Wet etching is a technique in which a substrate is immersed in a liquid etchant or subjected to a chemical solution that dissolves or reacts with specific materials. The etchant selectively removes the exposed material, leaving behind the desired pattern or structure.

Advantages:

- Offers excellent selectivity.
- Relatively simple and cost effective
- It can be easily scaled u to process large areas.
- It allows for control over the etch profile.

Disadvantages:

- Lack of precision as it is isotropic.

- Mask misalignment can lead to distorted patterns.
- It can cause undercutting.
- It involves handling and disposal of etchants, which may be corrosive, toxic, or hazardous.

II. Dry Etching:

Dry etching is a semiconductor fabrication technique that involves the removal of material from a substrate using gas-phase reactive species or physical bombardment. Unlike wet etching, which utilizes liquid etchants, dry etching is performed in a gas or plasma environment. It can be categorized into two main types: physical etching and chemical etching:

a) Physical Etching (Physical Sputtering): Physical etching, also known as physical sputtering, involves the bombardment of the substrate surface with energetic particles, such as ions or neutral atoms. These particles transfer momentum to the surface atoms, causing them to be physically ejected or sputtered away.

Advantages:

- Anisotropic Etching: Physical etching enables anisotropic material removal, allowing for precise control over feature dimensions and sidewall profiles.
- Directionality: The physical bombardment provides directional etching, resulting in vertical sidewalls and well-defined patterns.
- High Etch Rate: Physical etching processes can achieve high etch rates, facilitating fast material removal.
- Selectivity: Physical etching can exhibit selectivity by preferentially sputtering certain materials while leaving others unaffected.

Disadvantages:

- Mask Damage: Energetic particle bombardment can cause damage to the etch mask or the underlying layers, leading to mask erosion or degradation.
- Lateral Damage: Physical etching may result in lateral damage, such as ion scattering or implantation effects, which can affect the performance of nearby devices or structures.

- Limited Material Selectivity: Physical etching is generally less selective than chemical etching and may require additional steps to achieve the desired selectivity.

b) Chemical Etching (Chemical Reactions): Chemical etching involves the use of reactive gases or plasmas to chemically react with the material being etched, resulting in its removal. The etchant gases react with the surface material, forming volatile compounds that are subsequently removed from the substrate.

Advantages:

- Selectivity: Chemical etching offers high selectivity, allowing specific materials to be etched while leaving others intact. This selectivity enables precise pattern transfer and material removal.
- Isotropic and Anisotropic Etching: Chemical etching can be tailored to achieve either isotropic or anisotropic material removal, providing flexibility in creating different feature shapes.
- Material Compatibility: Chemical etching is compatible with a wide range of materials, including metals, oxides, nitrides, and polymers

Disadvantages:

- Mask Erosion: Some chemical etchants may attack and degrade the etch mask, leading to reduced pattern fidelity and compromised device performance.
- Etch byproducts: Chemical etching can generate byproducts that may deposit on the substrate, causing contamination or surface defects.
- Slow Etch Rates: Compared to physical etching, chemical etching processes often have lower etched rates, which can result in longer process times.

**Reactive Ion Etching**: Reactive Ion Etching (RIE) is a dry etching technique commonly used in semiconductor fabrication and other industries to precisely pattern and etch thin films or materials on a substrate. RIE involves the use of reactive gases and plasma to remove the material selectively, achieving high etching accuracy and control. In RIE, a low-pressure plasma environment is created in a vacuum chamber by applying a high-frequency electrical field to a gas mixture. The reactive gases typically used in RIE include a chemically active gas (e.g., oxygen, fluorine) and an inert gas (e.g., argon). The

plasma generated from the gas mixture contains ions, electrons, and reactive species that interact with the material to be etched.

## 3.7 Yield

Yield is a critical metric in semiconductor manufacturing, representing the effectiveness and efficiency of the process in producing functional devices that meet required specifications. A high yield indicates a high percentage of good devices, while a low yield suggests a higher rate of defects or failures.

To ensure the quality, reliability, and yield of the final products, defect inspection plays a vital role in semiconductor manufacturing. It involves detecting and identifying defects or anomalies in fabricated devices or wafers at various stages of the manufacturing process. Defect inspection aims to classify defects that could impact the performance, functionality, or reliability of semiconductor devices. By identifying process issues, equipment malfunctions, material defects, or design-related problems, defect inspection helps prevent low yield or device failures.

Defect Preview complements defect inspection by providing a quick and efficient way to identify potential defects on wafers or semiconductor devices. This preliminary assessment allows manufacturers to identify areas or regions that may contain defects or anomalies, leading to early detection of yield-limiting issues. Various techniques can be used for Defect Preview, including:

- Optical Inspection: Optical techniques, like bright-field microscopy or dark-field imaging, use visible or ultraviolet light to capture images of the wafer or device surface. This method quickly detects macroscopic defects such as scratches, particles, or pattern deviations.
- Scanning Electron Microscopy (SEM): SEM provides high-resolution images of the wafer or device surface, allowing closer examination of surface defects in the sub-micron range, such as line breaks or bridge connections.

By employing defect inspection and defect preview techniques, semiconductor manufacturers can optimize yield, enhance product quality, and address issues early in the manufacturing process, leading to more reliable and efficient semiconductor devices.

# Chapter – 4

# Fabrication Lab and their Products

## 4.1 Fabrication lab Working on Latest Technology

| Fabrication Lab | Technology | Latest Product | Products |
|---|---|---|---|
| Semiconductor Manufacturing International Corporation (SMIC) | 14nm, 12nm, 7nm | SMIC 7nm FinFET process | Mobile Processors, Image Sensor, RF Chips, Networking Chips |
| China National Semiconductor Corporation (CSSC) | 28nm, 16nm, 14nm | CSSC 16nm FinFET process | Mobile Processors, Image Sensor, RF Chips, Networking Chips |
| Tianjin University Microelectronics Institute (TUIMI) | 65nm, 40nm, 28nm | TUIMI 28nm FD-SOI process | Image Sensor, RF Chips, IOT Devices |
| Tsinghua University Microelectronics Institute (Tsinghua IME) | 14nm, 12nm, 7nm | Tsinghua IME 7nm FinFET process | Automotive chips, Industrial chips, Consumer electronics chips |
| Taiwan Semiconductor Manufacturing Company (TSMC) | 5nm, 3nm, 2nm | TSMC N5 process | Mobile Processors, Image Sensor, RF Chips, Networking Chips |
| United Microelectronics Corporation (UMC) | 7nm, 6nm, 5nm | UMC N7 process | Image sensors, RF chips, and Networking chips |
| MediaTek | 6nm, 5nm, 4nm | Dimensity 9000 chip | Laptops, Mobile |
| Powerchip Semiconductor | 40nm, 28nm, 22nm | PSMC 28nm FD-SOI process | Image Sensor, RF Chips |

| | | | |
|---|---|---|---|
| Manufacturing Corporation (PSMC) | | | |
| Intel | 10nm, 7nm, 5nm | Intel 7nm process | Processors |
| GlobalFoundries | 12nm, 10nm, 7nm | GlobalFoundries 12nm FinFET process | Mobile Processors, Image Sensor |
| IBM | 2nm, 1nm | IBM 2nm process | Mobile Processors, AI Chips |
| Samsung | 8nm, 7nm, 5nm | Samsung 5nm process | Mobile Processors, Image Sensor |
| TSMC | 16nm, 12nm, 7nm | TSMC N7 process | Apple A14 Bionic and the Snapdragon 865 (Mobile Processors), Automotive Chips |
| STMicroelectronics | 14nm, 12nm, 6nm | STMicroelectronics 12nm FinFET process | Image Sensor, RF Chips |
| Global Foundries | 12nm, 10nm, 7nm | GlobalFoundries 12nm FinFET process | Mobile Processors, Image Sensor, RF Chips, Networking Chips |
| Infineon Technologies | 16nm, 14nm, 12nm | Infineon Technologies 16nm FinFET process | Power management ICs, RF ICs, Security chips |

Table 4.1 – Fabrication Labs

## 4.2 Process Explanation

i. **SMIC 7nm FinFET process:**
The SMIC 7nm FinFET process is a semiconductor manufacturing process that was developed by Semiconductor Manufacturing International Corporation (SMIC). It is based on the FinFET transistor architecture, which allows for smaller transistors and higher transistor density than previous process nodes.

The SMIC 7nm FinFET process uses a number of advanced technologies, including:

- Extreme ultraviolet lithography (EUV) to pattern the transistors
- High-k metal gate (HKMG) to improve transistor performance
- Selective doping to control transistor characteristics

The SMIC 7nm FinFET process is capable of producing chips with a transistor density of up to 100 million transistors per square millimetre. This is significantly higher than the transistor density of previous process nodes, such as the 14nm FinFET process.

### ii. CSSC 16nm FinFET process

The CSSC 16nm FinFET process is a semiconductor manufacturing process that was developed by China Semiconductor Manufacturing (CSSC). It is based on the FinFET transistor architecture, which allows for smaller transistors and higher transistor density than previous process nodes.

The CSSC 16nm FinFET process uses a number of advanced technologies, including:

- High-k metal gate (HKMG) to improve transistor performance
- Selective doping to control transistor characteristics
- Stress engineering to improve transistor reliability

The CSSC 16nm FinFET process is capable of producing chips with a transistor density of up to 60 million transistors per square millimetre. This is significantly higher than the transistor density of previous process nodes, such as the 28nm FinFET process.

### iii. TUIMI 28nm FD-SOI process

The TUIMI 28nm FD-SOI process is a semiconductor manufacturing process that was developed by Tsinghua Unigroup Integrated Memory and IC Design Centre (TUIMI). It is based on the FinFET transistor architecture and uses fully depleted silicon on insulator (FD-SOI) technology.

FD-SOI technology has a number of advantages over traditional bulk CMOS technology, including:

- Reduced power consumption: FD-SOI transistors can be operated at lower voltages, which can lead to significant power savings.
- Improved performance: FD-SOI transistors can switch faster than bulk CMOS transistors, which can lead to improved performance.

- Increased flexibility: FD-SOI transistors can be scaled more easily than bulk CMOS transistors, which can lead to new opportunities for chip designers.

The TUIMI 28nm FD-SOI process is capable of producing chips with a transistor density of up to 45 million transistors per square millimetre. This is significantly higher than the transistor density of previous process nodes, such as the 40nm bulk CMOS process.

### iv. Tsinghua IME 7nm FinFET process

The Tsinghua IME 7nm FinFET process is a semiconductor manufacturing process that was developed by Tsinghua Unigroup Microelectronics (IME). It is based on the FinFET transistor architecture and uses extreme ultraviolet lithography (EUV) technology.

EUV technology is a key enabling technology for the 7nm process node. It allows for the patterning of transistors with features that are smaller than 10nm, which is necessary to achieve the desired performance and power efficiency.

The Tsinghua IME 7nm FinFET process is capable of producing chips with a transistor density of up to 100 million transistors per square millimeter. This is significantly higher than the transistor density of previous process nodes, such as the 14nm FinFET process.

### v. TSMC N5 process

TSMC N5 is a semiconductor manufacturing process that was developed by TSMC. It is based on the FinFET transistor architecture and uses extreme ultraviolet lithography (EUV) technology.

EUV technology is a key enabling technology for the 5nm process node. It allows for the patterning of transistors with features that are smaller than 10nm, which is necessary to achieve the desired performance and power efficiency.

The TSMC N5 process is capable of producing chips with a transistor density of up to 171 million transistors per square millimetre. This is significantly higher than the transistor density of previous process nodes, such as the 7nm FinFET process.

### vi. Dimensity 9000 Chips

The Dimensity 9000 is a mobile system-on-a-chip (SoC) manufactured by MediaTek using a 4nm process node. It was announced in November 2021 and is the first commercial SoC to use the Armv9 architecture.

The Dimensity 9000 features an octa-core CPU with one Arm Cortex-X2 core clocked at up to 3.05 GHz, three Arm Cortex-A710 cores clocked at up to 2.85 GHz, and four Arm Cortex-A510 cores clocked at up to 2.0 GHz. It also features a Mali-G710 MC10 graphics processor, a 18-bit image signal processor (ISP), and a 5G modem.

The Dimensity 9000 is designed for flagship smartphones and is expected to offer significant performance improvements over previous-generation SoCs. It is also expected to be more power-efficient, thanks to the Armv9 architecture and the 4nm process node.

## vii. PSMC 28nm FD-SOI process

The PSMC 28nm FD-SOI process is a semiconductor manufacturing process that was developed by STMicroelectronics (STM). It is based on the FinFET transistor architecture and uses fully depleted silicon on insulator (FD-SOI) technology.

FD-SOI technology has a number of advantages over traditional bulk CMOS technology, including:

- Reduced power consumption: FD-SOI transistors can be operated at lower voltages, which can lead to significant power savings.
- Improved performance: FD-SOI transistors can switch faster than bulk CMOS transistors, which can lead to improved performance.
- Increased flexibility: FD-SOI transistors can be scaled more easily than bulk CMOS transistors, which can lead to new opportunities for chip designers.

The PSMC 28nm FD-SOI process is capable of producing chips with a transistor density of up to 45 million transistors per square millimeter. This is significantly higher than the transistor density of previous process nodes, such as the 40nm bulk CMOS process.

## viii. Intel 7nm process

Intel's 7nm process is a semiconductor manufacturing process that was originally scheduled to be released in 2018. However, there were a number of delays, and the process is not expected to be commercially available until 2023.

The Intel 7nm process is based on the FinFET transistor architecture and uses extreme ultraviolet (EUV) lithography. EUV is a key enabling technology for the 7nm process node, as it allows for the patterning of transistors with features that are smaller than 10nm.

The Intel 7nm process is expected to offer a number of advantages over previous process nodes, such as smaller transistors, increased transistor density, and improved performance and power efficiency.

## ix. GlobalFoundries 12nm FinFET process

The GlobalFoundries 12nm FinFET process is a semiconductor manufacturing process that was developed by GlobalFoundries. It is based on the FinFET transistor architecture and uses extreme ultraviolet (EUV) lithography.

EUV technology is a key enabling technology for the 12nm process node, as it allows for the patterning of transistors with features that are smaller than 10nm.

The GlobalFoundries 12nm FinFET process is capable of producing chips with a transistor density of up to 100 million transistors per square millimeter. This is significantly higher than the transistor density of previous process nodes, such as the 14nm FinFET process.

**x. IBM 2nm process**

The IBM 2nm process is a semiconductor manufacturing process that was developed by IBM. It is based on the gate-all-around (GAA) transistor architecture and uses extreme ultraviolet (EUV) lithography.

GAA technology is a new transistor architecture that is expected to offer a number of advantages over traditional FinFET transistors, such as improved performance and power efficiency. EUV technology is a key enabling technology for the 2nm process node, as it allows for the patterning of transistors with features that are smaller than 5nm.

The IBM 2nm process is capable of producing chips with a transistor density of up to 500 million transistors per square millimeter. This is significantly higher than the transistor density of previous process nodes, such as the 7nm FinFET process.

## 4.3 Fabrication Lab Working on 90nm and 180nm

| Fab | Location | Products | Process Node |
|---|---|---|---|
| TSMC | Taiwan | AIoT chips, automotive chips, networking chips | 180nm |
| GlobalFoundries | Singapore | Networking chips, industrial chips | 180nm |
| SMIC | China | Smart home chips, automotive chips | 180nm |
| UMC | Taiwan | Networking chips, industrial chips | 180nm |
| TowerJazz | Israel | RF chips, image sensors | 180nm |
| TSMC | Taiwan | Low-power microcontrollers | 90nm |
| GlobalFoundries | Singapore | Networking chips, industrial chips | 90nm |
| SMIC | China | Smart home chips, automotive chips | 90nm |
| UMC | Taiwan | Networking chips, industrial chips | 90nm |

Table 4.2 – Fabrication Lab for 180nm and 90nm node

## 4.4 Products:

### i. AIoT chips

AIoT chips are a type of semiconductor that is designed for use in artificial intelligence (AI) and the internet of things (IoT). They are typically based on the latest process nodes and technologies, and they are designed to be energy-efficient and powerful. AIoT chips are used in a wide range of applications, including self-driving cars, smart homes, and industrial automation.

### ii. Automotive chips

Automotive chips are a type of semiconductor that is specifically designed for use in vehicles. They are used in a wide range of applications, including:

- Engine control: Automotive chips control the engine's performance, including fuel efficiency, emissions, and power delivery.
- Safety: Automotive chips are used in a variety of safety features, such as anti-lock braking systems (ABS), electronic stability control (ESC), and airbags.
- Infotainment: Automotive chips power the infotainment system, which includes the radio, navigation, and entertainment features.
- Connectivity: Automotive chips enable connectivity features, such as Bluetooth, Wi-Fi, and cellular data.

### iii. Networking chips

Networking chips are a type of semiconductor that is specifically designed for use in networking applications. They are used in a wide range of devices, including:

- Routers: Networking chips power the routers that route data packets across networks.
- Switches: Networking chips power the switches that connect devices on a network.
- Firewalls: Networking chips power the firewalls that protect networks from unauthorized access.
- Wireless access points: Networking chips power the wireless access points that allow devices to connect to a network wirelessly.

### iv. Industrial chips

Industrial chips are a type of semiconductor that is specifically designed for use in industrial applications. They are used in a wide range of devices, including:

- Programmable logic controllers (PLCs): Industrial chips power the PLCs that control industrial machinery.
- Sensors: Industrial chips power the sensors that monitor industrial processes.
- Actuators: Industrial chips power the actuators that control industrial machinery.
- Embedded systems: Industrial chips are used in a variety of embedded systems, such as those used in factory automation and robotics.

### v. RF chips

RF chips are integrated circuits (ICs) that are specifically designed to operate at radio frequencies (RF). They are used in a wide variety of applications, including cell phones, wireless networks, Bluetooth devices, Wi-Fi devices, and radar systems.

RF chips are typically made using a process called complementary metal-oxide semiconductor (CMOS). CMOS is a type of semiconductor technology that is well-suited for RF applications because it can be used to create small, efficient, and reliable chips.

RF chips contain a number of different components, including:

- A transmitter: The transmitter converts digital signals into radio waves.
- A receiver: The receiver converts radio waves into digital signals.
- An antenna: The antenna is used to transmit and receive radio waves.
- A control unit: The control unit manages the operation of the RF chip.

RF chips are a critical component of many electronic devices. As the use of wireless technologies continues to expand, the demand for RF chips is expected to grow significantly in the coming years.

**vi. Image sensors**

An image sensor is a type of semiconductor that is used to convert light into electrical signals. It is used in a wide variety of applications, including digital cameras, smartphones, and security cameras.

Image sensors typically contain a grid of pixels, each of which is a tiny light sensor. When light hits a pixel, it creates an electrical charge. The amount of charge created is proportional to the amount of light that hit the pixel.

The electrical charges from the pixels are then amplified and converted into digital signals. These digital signals are then stored in memory or transmitted to a computer or other device.

Here are some of the key features of image sensors:

- Resolution: The resolution of an image sensor is the number of pixels that it contains. The higher the resolution, the more detailed the image will be.
- Sensitivity: The sensitivity of an image sensor is how well it can detect light. The more sensitive an image sensor is, the better it will be able to take pictures in low-light conditions.
- Dynamic range: The dynamic range of an image sensor is the range of brightness that it can capture. The wider the dynamic range, the better the image sensor will be able to capture both bright and dark areas in a scene.
- Noise: Noise is unwanted electrical signals that can be present in an image sensor's output. Noise can degrade the quality of an image.

**vii. Low-power microcontrollers**

A low-power microcontroller is a type of microcontroller that is designed to consume less power than a traditional microcontroller. This is achieved by using a number of techniques, such as:

- Power-saving modes: Low-power microcontrollers typically have a number of power-saving modes that can be used to reduce power consumption when the microcontroller is not actively processing data.
- Low-leakage transistors: Low-power microcontrollers use transistors that have low leakage current, which helps to reduce power consumption when the microcontroller is in standby mode.
- Asynchronous operation: Low-power microcontrollers can often be operated in asynchronous mode, which means that they do not need to be clocked by an external clock source. This can further reduce power consumption.

# Chapter 5

# Project

## EXPERIMENTAL ANALYSIS OF MOS CAPACITOR FOR OXIDE FURNACES BY USING CV PLOTTER METROLOGY

### 5.1 Introduction:

Capacitance Voltage (CV) analysis is a fundamental technique used to characterize the electrical properties of a Metal-Oxide-Semiconductor (MOS) capacitor. MOS capacitors are essential building blocks of modern electronic devices, particularly in integrated circuits. Understanding their behaviour and characteristics is crucial for designing and optimizing semiconductor devices. This report presents an overview of the Capacitance Voltage analysis technique and its application to MOS capacitors.

### 5.2 MOS Capacitor Basics:

A MOS capacitor is formed by sandwiching a thin insulating layer, typically silicon dioxide ($SiO_2$), between a metal electrode and a semiconductor substrate, often silicon. The metal electrode is referred to as the gate, the insulating layer as the oxide, and the semiconductor substrate as the body. The voltage applied to the gate terminal controls the amount of charge stored in the oxide, modulating the capacitance of the MOS structure.

### 5.3 Capacitance Voltage Analysis:

CV analysis is a non-destructive method used to measure the capacitance as a function of the applied voltage across the MOS capacitor. The key principle behind CV analysis is that the capacitance of the MOS structure is inversely proportional to the thickness of the oxide layer and directly related to the charge stored in it.

### 5.4 Experimental Setup:

The CV analysis typically involves the following steps:

1. Fabrication of MOS capacitors on a silicon wafer.

2. Application of a voltage sweep to the gate terminal.

3. Measurement of the resulting capacitance at each voltage point.

### 5.5 CV PLOTTER:

- Equipments Role and Description

  Model: MDC CV Plotter

  Basic Configuration:

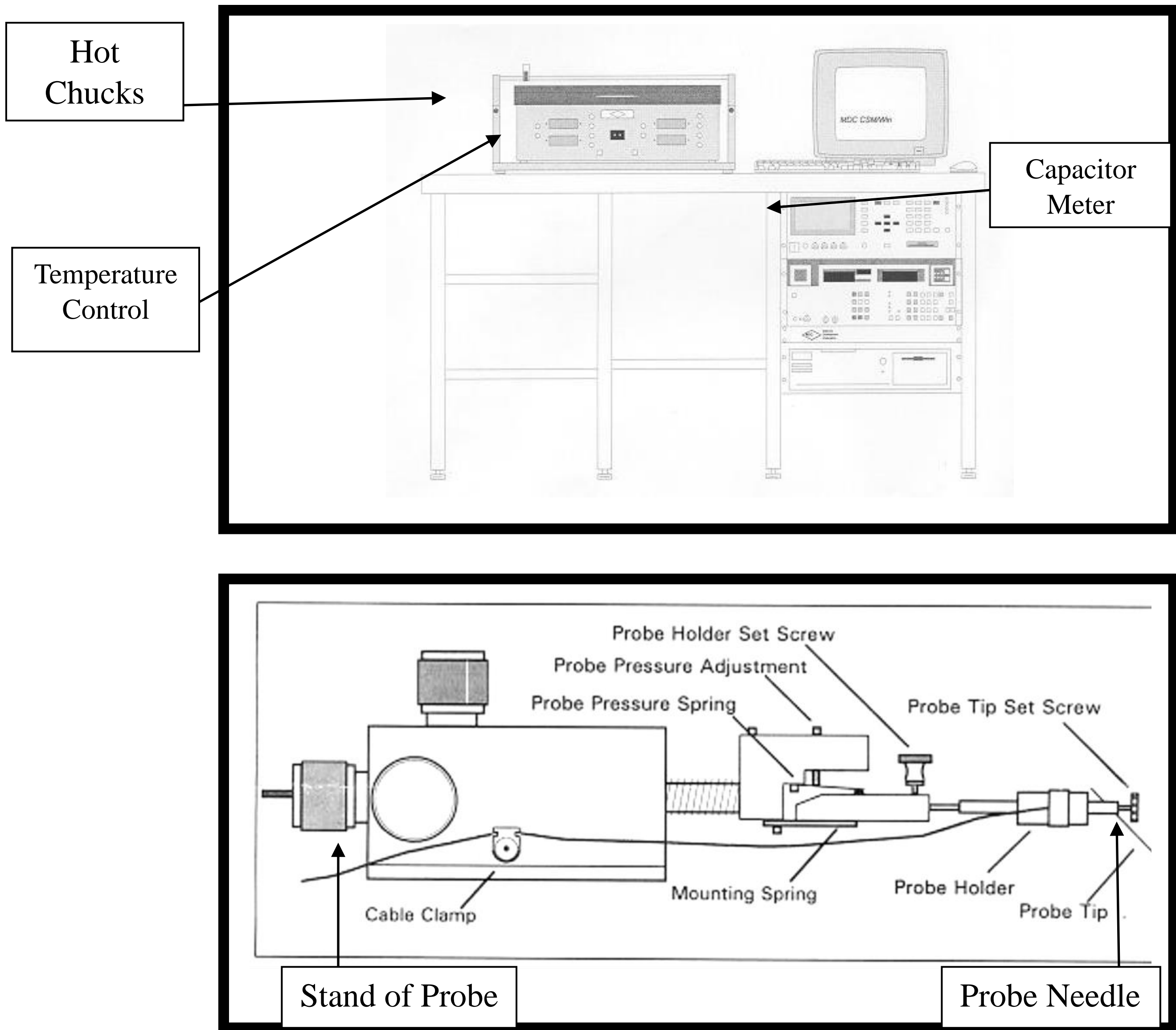



Figure 5.1- CV Plotter

- Principle of Measurement: This equipment is measuring the Mobile Ion concentration in the process equipment. The test is part of furnace qualification.

Purpose and Principle of operation

- This machine measures Mobile Ion concentration potassium and sodium, in oxide.
- The measurement goal is to check clean level of furnaces. Measure the mobility ion of oxide film in order to verify cleanses of environment inside of tube.
- The flatband voltage of real MOS structures is further affected by the presence of charge in the oxide or at the oxide semiconductor interface. The

flatband voltage still corresponds to the voltage, which, when applied to the gate electrode, yields a flat energy band in the semiconductor. Any charge in the oxide or at the interface affects the flatband voltage.

$$V_{FB} = \varphi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x \, dx$$

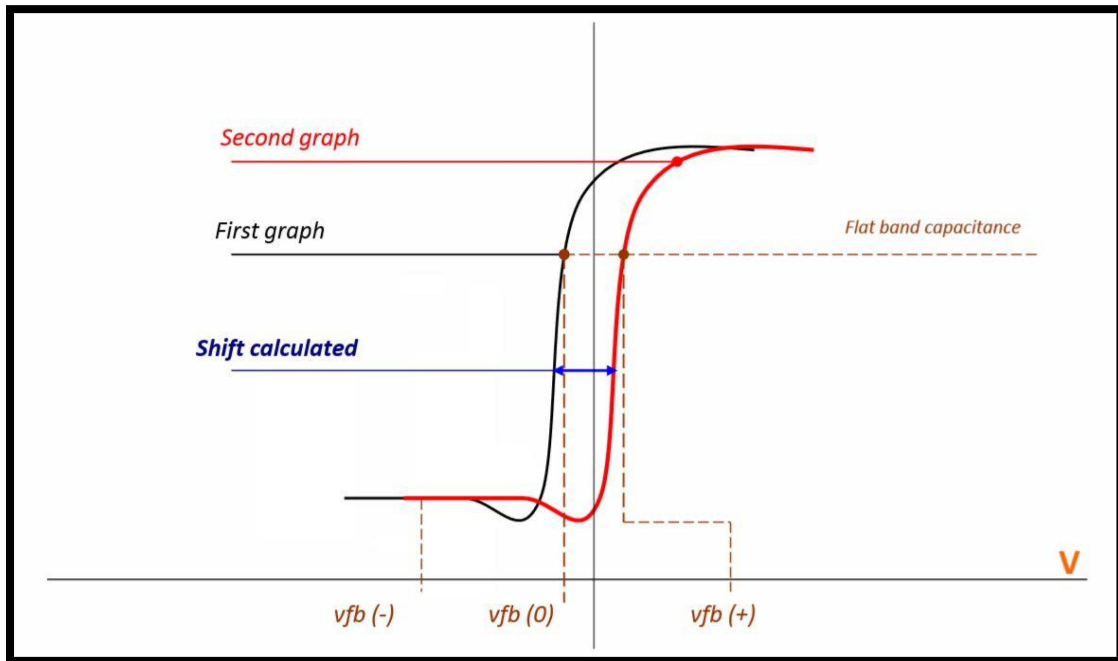



Figure 5.2 – CV Plot

Procedure for CV Plotter:

- The wafer is kept on the chuck inside the black box. Probe is connected using a microscope parallel to the Anode part of the made MOS capacitor.
- MDS CSM/Win System is open, and we run the Experimental Analysis. We choose the recipe. Capacitance meter is made zero and black box is closed now. Voltage is varied from -5V to 5V with an increase of 0.1V. The process is executed at 35˚C.The following

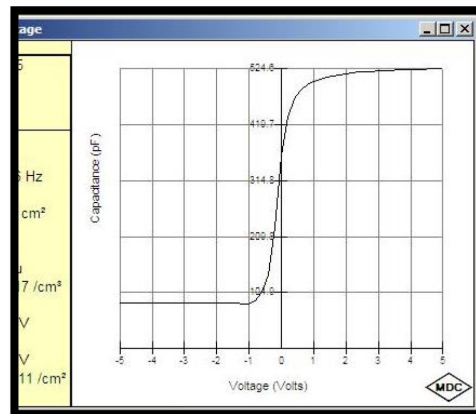



Figure 5.3 – Graph Obtained 1

Output is satisfactory, so we move to Production Analysis and plot the graph.

- We run Production Analysis. We choose the defined recipe and then process is carried out. First the voltage is varied from -5V to 5V at 37°C and then wafer is heated to 290°C at fixed bias of 5V.
- After that wafer is kept at 290°C for 3 minutes (Soak Time) and cooled to 37°C.
- Voltage is varied from -5V to 5V again and graph is obtained. Graph tells us about the variation in CV graph before and after heating. $V_{fb}$ is calculated, if it is within limits then the wafer is under control limit.
- Graph obtained is as follows:

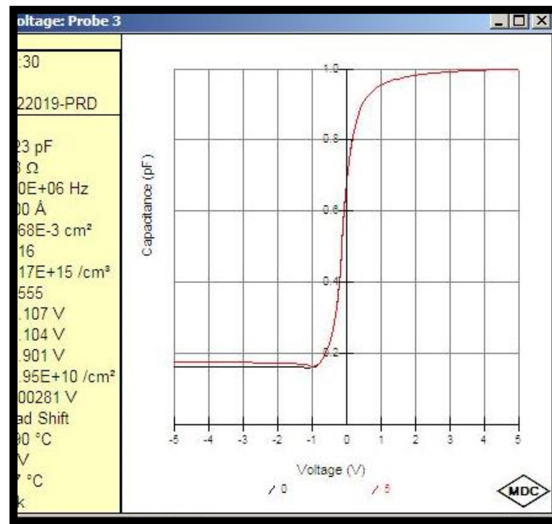



Figure 5.4 – Graph Obtained 2

$V_{fb}$ in this case is 0.00281V. Though shift is bad but the change in CV graph before and after heating is negligible.

Thence the given MOS is under control limits and the furnace has less contamination.

### 5.6 Accumulation, Depletion, and Inversion Regions:

During the voltage sweep, the MOS capacitor goes through different regions based on the voltage applied to the gate:

- Accumulation Region: When a negative voltage is applied to the gate, electrons are attracted to the oxide-semiconductor interface, resulting in the accumulation of charge and an increase in capacitance.
- Depletion Region: At slightly positive voltages, the semiconductor surface gets depleted of majority carriers (holes in p-type and electrons in n-type), leading to a decrease in capacitance.
- Inversion Region: With further increasing the gate voltage positively, the surface can invert, attracting carriers opposite to the substrate type. In this region, the capacitance starts increasing again.

### 5.7 CV Analysis and Device Parameters:

CV analysis provides valuable information about the MOS capacitor and the semiconductor material, such as:

- Flat band Voltage (V_fb): The voltage at which the capacitance is minimum, and the semiconductor is in the depletion region.
- Threshold Voltage (V_th): The voltage at which the surface is inverted, and the MOS capacitor starts conducting.
- Oxide Thickness (tox): Determined by measuring the capacitance at different frequencies and calculating the oxide capacitance.

### 5.8 Process flow of MOS (Metal Oxide Semiconductor):

- Process: Gate Oxide CV Furnace Qualification (CV for Furnace)
- LOT ID: SC19160001.F1
- Purpose: CV for FRGO1
- **Step1:** Test wafer is taken, having properties: Material – Silicon, Doping – n-Type. So now the n type substrate is taken for next step.
- **Step 2:** The wafer is taken to Laser mark section, where LOT ID of wafer is printed on it using Laser. The tool we use to embark LOT ID on wafer is SLSM1. Format of printing will be FYYWWNNNN-XX, where FYYWWNNNN signifies the LOT Number and XX signifies the Wafer Number. The mark is orientated at 90˚ to the notch (Recipe: Product-SCL.Job.
- **Step 3:** Wafer is now cleaned, which is known as Pre Diffusion Clean. It is done to clean of the impurities (mainly metallic) present over the wafer. It is carried out in tool - WTPD1 for 12 hr (Recipe: PRECLN).
- **Step 4:** Now the very first layer i.e. Oxide layer is formed over the surface using the process of Diffusion (Oxidation). The gases involved are $O_2$ and $N_2$. This is carried out in FRST1 at 1000˚C. $SiO_2$ is formed with thickness of 500Å with an error available of 50Å. (Recipe: /SCL/CV500 AA-OX)

- **Step 5:** Then the wafer is to taken to the Diffusion metrology tool: Ellipsometer. It can provide both film thickness and index of refraction information. In an ellipsometer a laser beam is elliptically polarized and reflected from the specimen to be measured. The reflected beam passes through an analyzer drum and onto a detector. The analyzer drum is rotated to produce a minimum value in the light intensity reaching the photo detector. By reading the polarizer and analyzer settings the film thickness and index of refraction may be read.

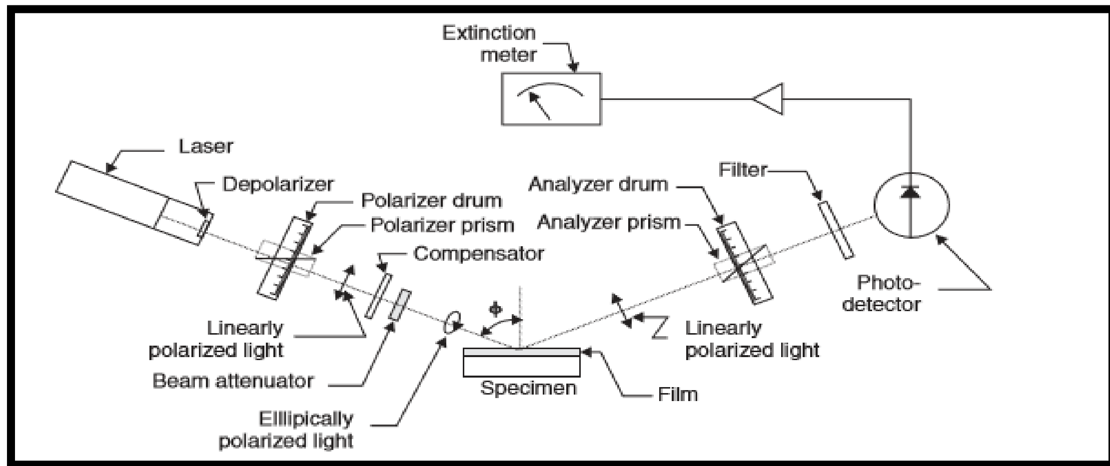



Figure 5.5 –Schematic of Ellipsometer

- Process name is CV THICKNESS; it is carried out in MTRU1. Recipe used is SCL_Thin. Thickness is measured as:

| Parameter Name | Wafer No. | Site | Value | Unit | CMIN | CMAX | SMIN | SMAX |
|---|---|---|---|---|---|---|---|---|
| CV500Thick_Mean | 1 | Full | 523.8 | Angstrom | 450 | 600 | 450 | 600 |
| CV500Thick_Mean | 2 | Full | 5410.22 | Angstrom | 450 | 600 | 450 | 600 |
| CV500Thick_Mean | 3 | Full | 508.83 | Angstrom | 450 | 600 | 450 | 600 |
| CV500Thick_Mean | 4 | Full | 521.6 | Angstrom | 450 | 600 | 450 | 600 |
| CV500Thick_Unif | 1 | Full | 2.67 | Percentage | 450 | 600 | 450 | 600 |
| CV500Thick_Unif | 2 | Full | 1.78 | Percentage | 0 | 999 | 0 | 999 |
| CV500Thick_Unif | 3 | Full | 0.58 | Percentage | 0 | 999 | 0 | 999 |
| CV500Thick_Unif | 4 | Full | 3.77 | Percentage | 0 | 999 | 0 | 999 |

Table 5.1 – Parameter with Obseration

- **Step 6:** Then wafer is taken for cleaning. CVBACKSTRIP – Backside oxide (dry oxide, 500Å) is cleaned in this process using wet etching. This process is carried in WTSE1 and recipe used is CCD BHF650.

- **Step 7:** Inspection is done next. CV500ColorINS – [Backside Visual Inspection (Macro), Thermal Oxide, Thickness=500Å] is done. It is done manually. It is done in YEOI1 by the tool engineer.
- **Step 8:** After Oxide, it is now turn for Metal to be deposited. CVMETAL – CV Metal Sputter is done. AlCu is deposited over the oxide layer using Sputtering. A layer of 8000Å is deposited in which 0.5% is Cu with Control limit of$\pm$800Å. It is done in Tool – SPAL1 using Template No. 55.
- **Step 9:** After Metal deposition. For creating isolated MOS, A Photo resist layer with particular pattern is made over the metal surface. CVMETALPHOT - M3 PHOTO DUV means M3 mask is used to create pattern in DUV1 Equipment.
- **Step 10:** DICD measurement is done after photoresist.
- **Step 11:** Now manual Visual Inspection is done: it is done in YEOI1 by the tool engineer to check for any contamination.
- **Step 12:** Now metal is etched using process CV Metal Etch. AlCu is etched 8000Å in dry etch area. The process is carried in REML1 using recipe Z-CV-AL-8000A.
- **Step 13:** After etching the metal. We remove the remaining Photo resist layer by ashing it. Metal is ashed in ASBE1 following recipe Al-ASHER-60.
- **Step 14:** After ashing the wafer is cleaned using Polymer to remove photo resist if any. It is done in WTSL1 using recipe M REMOVE-1 in Wet Etch area.
- **Step 15:** Now the Top metal layer is annealed to remove its stress. It is done in FRAN1 at 450°C in presence of $N_2$ and $H_2$ gas for 30 minutes using recipe: D1-TEOS-Anneal.
- **Step 16:** Now we check the CV qualification of the MOS device created using CV Plotter (MTCV1).

### 5.9 Applications:

CV analysis has numerous applications in semiconductor device characterization and process development. Some of its common applications include:

- Extracting doping concentration and interface trap density.
- Evaluating the quality of the insulating oxide layer.
- Characterizing the behaviour of high-k dielectrics used in advanced devices.
- Monitoring the effects of process variations on device performance.

# Chapter 6 - Conclusion

In conclusion, this study delved into the domain of VLSI fabrication and sought to identify key fabrication labs in China, Taiwan, USA, and Europe. Through a thorough examination of these regions' capabilities and technological advancements, the research revealed valuable insights into their competitive positions within the semiconductor industry. The findings showcased the varied strengths and weaknesses of each region, offering essential information for policymakers and industry stakeholders to make informed decisions regarding collaboration, investment, and strategic partnerships.

In this project, the contamination level of furnace was inspected by analysing a MOS capacitor with oxide layer of 500A. This contamination level will be tested by measuring Capacitance-Voltage characteristics of the MOS Capacitor in the metrology tool MTCV1 CV Plotter. The tools' purpose is to monitor the environment of diffusion oxide furnaces and maintain the quality control of the furnace. The Charge $Q_m$ gets activated after temperature >100°C and gets trapped in Oxide Transition region. So, this cause later shift in the second CV plot with respect to the first. To check sensitivity of we use 500A thick oxide layer. If contamination is high then the difference in the graphs will be more. The measurement produces two Capacitance-Voltage graphs, first one measure the Capacitance-Voltage relation at room temperature 35°C, and then it is heated to 290°C & kept at 290°C for three minutes and cooled to 35°C to test whether it will work properly when used again and again (as when it is used the temperature of operation is quite high too >100°C). Second Graph is plotted again, this tells the deviation in the CV characteristics of the device due to contamination present in it while diffusion.

The results should be lower (value of $V_{fb}$ should be within the control limits of the device i.e. +0.2V >= $V_{fb}$ >= -0.2V for 500Å oxide layer). In our case value of Flatband Voltage $V_{fb}$ is 0.00281V which in within control limit. This indicates that contamination of metal impurities in the furnace is negligible. The measurement can be done several times on wafer in other structure, in any die.

Overall, the combination of the comparative analysis of VLSI fabrication facilities and the CV analysis for MOS capacitors enables a comprehensive understanding of the technological landscape and potential advancements in the semiconductor industry. By promoting international cooperation and sharing best practices, this research fosters a collaborative environment that can drive innovation and facilitate progress in the ever-evolving world of VLSI technology. The study's outcomes serve as a foundation for future research and development, laying the groundwork for a more interconnected and thriving semiconductor ecosystem that benefits global society as a whole.